IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **M. Takada, H. Minoura, K. Tsukada, H. Kobayashi and M. Kondo**

Application No.:09/380,994 Examiner: **R. Bekkering**

Filing Date: **September 13, 1999** Group Art: **2841**

Title: **PRINTED WIRING BOARD AND METHOD FOR MANUFACTURING SAME**

CERTIFICATE OF MAILING

I hereby certify that this correspondence, along with any papers indicated as being deposited as first class mail in an envelope addressed to: Commissioner for Patents, Washington D.C. 20231 on July 19, 2002.

7.19.02
Date

Denise Grisack

Commissioner for Patents
Washington, DC 20231

RESPONSE TO OFFICE ACTION DATED February 19, 2002

Sir:

In the Claims

Please amend the claims as follows:

Please amend claim 1 as follows:

1. (Twice Amended) A printed wiring board comprising an odd number n of conductive layers which are built up with a same odd number of insulating layers, respectively, and are electrically connected to one another via interconnecting through holes;

D1

wherein a first conductive layer on which an electronic component layer is to be mounted and conducts electric currents in and out of the electronic component; an n-th conductive layer is an external connecting layer for connecting external connecting terminals which conduct electric

currents in and out of the printed wiring board; a second to (n-1)-th conductive layers are current transmitting layers for transmitting internal currents of the printed wiring board; and a surface of the n-th conductive layer is covered with an n-th and outermost insulating layer with external connecting terminals being exposed, and wherein a central insulating layer of the odd number of insulating layers prevents warping from occurring in the printed wiring.

cont'd D1

Please amend claim 3 as follows:

3. (Thrice Amended) A method of manufacturing a printed wiring board having an odd number n of conductive layers which are built up with a same odd number of insulating layers, respectively, and are electrically connected to one another by first interconnecting through holes, the method comprising the steps of:

interposing the insulating layers between a second to n-th conductive layers, respectively, and also forming first interconnecting through holes for electrically connecting the conductive layers to one another;

D2

laminating a first prepreg and a copper foil on a surface of the second conductive layer, and press-bonding a second prepreg on a surface of the n-th conductive layer to form a multilayer substrate having an odd number n of insulating layers, wherein the second to n-th conductive layers are internal layers of the multilayer substrate;

etching the copper foil to form a first conductive layer;

forming second interconnecting through holes in a first insulating layer and forming connecting holes in an n-th insulating layer, respectively;

forming a metal plating film for electrically connecting a first conductive layer with the second conductive layer on the walls of the second interconnecting through holes of the first insulating layer; and

connecting external connecting terminals to a surface of the n-th conductive layer exposed through the first connecting through holes of the n-th insulating layer.

Contd D2

Please amend claim 4 as follows:

4. (Thrice Amended) A printed wiring board comprising an internal insulating substrate having a conductor circuit formed on a surface thereof, an internal insulating layer laminated on the surface of the internal insulating substrate, and an external insulating layer laminated on a surface of the internal insulating layer, the internal insulating layer and the external insulating layer having an internal conductor circuit and an external conductor circuit, respectively:

wherein the internal insulating layer comprises two or more internal insulating layers of glass cloth-reinforced prepreg containing 30 to 70% by weight of glass cloth.

Please amend claim 7 as follows:

7. (Amended) A method of manufacturing a printed wiring board having a plurality of conductive layers which are built up with insulating layers respectively and are electrically connected to one another by interconnecting through holes, the method comprising the steps of:

forming conductive layers on a plurality of insulating layers respectively;

laminating and press-bonding the resulting insulating layers to form a multilayer substrate;

irradiating a laser beam on the multilayer substrate at interconnecting through hole-forming portions to define interconnecting through holes with bottoms defined by the conductive layers;

cont'd D3

covering the walls of the interconnecting through holes with metal plating films; and fusing solder balls against the interconnecting through holes and filling them with solder.

Please cancel claim 11.

Please cancel claim 14.

Remarks

Applicant respectfully thanks the Examiner for the indication that claims 15 and 18 are allowed. The remaining claims, claims 1-4, 7, 10, 11, and 14, have been rejected based on prior art grounds. In addition, the Patent and Trademark Office (Office) has objected to claim 1 because, in line 5, "later" should be --layer--. Applicant also has amended claim 4 to add the limitation that the glass cloth-reinforced prepreg contains "30 to 70% by weight of glass cloth". Finally, Applicant has cancelled claims 11 and 14. Applicant has made additional amendments in claim 1, 3, 4, and 7 to correct additional typographical, grammatical and clerical errors and to improve their form. Accordingly, claims 1-4, 7, 10, 15 and 18 are now pending in this case.

The Office rejected claims 1 and 2 under 25 U.S.C. §102(e) as anticipated by Mizumoto. Particularly, the Office asserted that Figures 3 and 9 and column 4, lines 58-63, column 5, lines 9, 19-20, and 53-60 of Mizumoto disclose a board with five layers of insulation interconnected by through holes. According to the Office, "the first layer is a component connecting layer, the nth is an external layer, and layer n-1 are current transmitting", and "the nth layer is covered by an outermost insulating layer with the terminals exposed". The Office further asserted that the

central layer prevents warpage and that the external connecting terminals are solder balls as seen in Figure 3.

Applicant respectfully traverses this rejection.

The present invention as recited in claim 1 relates to a built up printed wiring board (PWB) having an odd number n of conductive layers such that the middle layer, i.e., layer number (n+1)/2, is in the center of the stack and has the same number of insulating layers above it and below it. This prevents warping of the PWB during press bonding of prepregs for forming the insulating layers. Further, the surface of the nth conductive layer is covered with the nth and outermost insulating layer, with the external connecting terminals being exposed. In other words, the PWB has the same, odd number of conductive layers as insulating layers and the last conductive layer is covered with the last insulating layer with the external connecting terminals exposed.

It appears that the Office has either misinterpreted Mizumoto or claim 1 of the present application because Mizumoto does not disclose the invention as claimed in claim 1. Actually, Mizumoto is very similar to the prior art described in the Background section of the present application in that it has an even number of conductive layers on an odd number of insulating layers, contrary to the claimed odd number of both insulating layers and conductive layers claimed in claim 1. The Office's assertion that the nth conductive layer is covered by an outermost insulating layer is incorrect. In Mizumoto, the nth conductive layer is exposed. It is not covered with an nth insulating layer. Particularly, see column 5, line 2 of Mizumoto, which states that layers 13 and 14 are surface laminar circuit (SLC) layers. Figure 4 shows a detail of SLC layer 13. As disclosed in column 5, lines 14-17, SLC layer 13 comprises two layers, including an insulation layer 26. Insulation layer 26 is the inner layer of SLC layer 13, not the outer layer.

Accordingly, contrary to the Office's assertion, Mizumoto does not teach equal numbers of conducting and insulating layers with the uppermost conducting layer covered with an uppermost insulating layer.

Claim 1 clearly distinguishes over Mizumoto. Particularly, claim 1 recites " a printed wiring board comprising an odd number n of conductive layers which are built up with an odd number of insulating layers respectively" and "the n-th conductive layer is covered with the n-th and outermost insulating layer with external connecting terminals being exposed". These limitations are not found in Mizumoto, which, as noted above, discloses a prior art PWB with an even number of conductive layers and an odd number of insulating layers with the nth conductive layer exposed. Accordingly, claim 1 clearly distinguishes over the prior art of record. Since claim 2 depends from claim 1, it distinguishes over the prior art of record for the same reasons.

The Office also rejected claims 3-4, 7 and 10 under 35 U.S.C.§ 103(a) as obvious over Mizumoto.

Applicant respectfully traverses these rejections also.

Claim 3 is an independent claim that distinguishes over the prior art of record for all of the same reasons discussed above in connection with claim 1. Particularly, claim 3 recites a method of manufacturing printed wiring board having "an odd number n of conductive layers which are built up with an odd number of insulating layers respectively", "press bonding a second prepreg on a surface of the n-th conductive layer to form a multi layer substrate having an odd number n of insulating layers, wherein the second to n-th conductive layers are internal layers of the multi layer substrate", and "connecting external connecting terminals of the surface of the surface of the n-th conductive layer exposed through the connecting holes of the n-th insulating layer". Since Mizumoto's printed circuit board has an exposed n-th conductive layer, it obviously does not meet any of these limitations.

Claim 4 is another independent claim in which a primary claimed feature is that a glass cloth-reinforced prepreg constitutes the internal insulating layer. Since the internal insulating layer contains glass cloth, the coefficient of water absorption can be reduced in the layer. Accordingly, the coefficient of water absorption of the internal insulating layer as a whole can be reduced.

In rejecting this claim as obvious over Mizumoto, the Office conceded that Mizumoto does not teach this feature. However, the Office asserted, without citing support, that it would have been obvious to use glass cloth prepreg to form the layers of the substrate in Mizumoto because use of glass cloth prepreg for this purpose is well known in the art.

Applicant respectfully traverses and has amended claim 4 to add the limitation that the prepreg contains 30 to 70 % by weight of glass cloth. Using a prepreg containing 30 to 70% by weight of glass cloth is not well known in the art. This range is particularly beneficial because prepregs that contain less than 30% by weight of glass cloth have high coefficients of water absorption and, therefore, are liable to undergo inter-layer delamination. On the other hand, prepregs with more than 70% by weight of glass cloth are likely to show low inter-layer adhesion since the absolute amount of resin is small. Accordingly, claim 4 does, in fact, distinguish over the prior art of record. Applicant having traversed this rejection, the Examiner must now withdraw the objection or cite a supporting reference. MPEP § 2144.03 (p2100-103, left column, top).

Claim 7 is an independent claim in which a primary claim feature is that after the insulating layers are laminated, a laser beam is used to form interconnecting through holes in the PWB. Accordingly, the interconnecting through holes, which penetrate all of the insulating layers, are formed by a single hole-defining procedure.

In rejecting claim 7 as obvious over Mizumoto, the Office conceded that Mizumoto does not teach forming the through holes with a laser beam. Nevertheless, the Office asserted, without citing a supporting prior art reference, that it would have been obvious to do so because such manufacturing methods were well known and routine in the art.

Applicant respectfully traverses the Examiner's assertion that forming through holes having bottoms with a laser beam is well known and routine in the art. Particularly, Mizumoto discloses only forming through holes by drilling (see column 5, lines 57-58). Further, claim 7 expressly recites "irradiating a laser beam on the multi layer substrate at interconnecting through hole-forming portions to define interconnecting through holes with bottoms defined by the conductive layers". Applicant disputes that forming through holes having bottoms with a laser beam is well known and routine in the prior art.

Applicant, having traversed the Office's assertion that this is know in the prior art without citing a supporting reference, the Office must now withdraw the rejection or cite the reference supporting this assertion. MPEP § 2144.03

Claim 10 depends from claim 7 and therefore, distinguishes over the prior art of record for all of the reasons discussed above in connection with claim 7.

Finally, the Office rejected claim 11 as anticipated by Feilchenfeld et al. and rejected dependent claim 14 as obvious over Feilchenfeld as applied to claim 11 and further in view of Glenn et al.

Applicant has herein cancelled these two claims, thus rendering this rejection moot.

As noted above, claims 15 and 18 have been indicated as allowable.

In view of the foregoing amendments and remarks, this application is now in condition for allowance. Applicant respectfully requests the Examiner to issue a Notice of Allowance at the

earliest possible date. The Examiner is invited to contact Applicant's undersigned counsel by telephone call in order to further the prosecution of this case in any way.

Respectfully submitted,

Dated: _____

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